In the Claims

Please cancel claims 2 and 11, and amend claims 1, 3-5. 9, 10, and 12, as set forth in the following listing of all claims in the application.

CLAIMS LISTING

1. (currently amended) A method for trimming a circuit device containing trim elements, the method comprising:

applying, in an online mode of operation, one or more trim bit sequences to the circuit device;

evaluating, in said online mode of operation, the effect on the circuit device resulting from each of the trim bit sequences applied thereto, without physically altering any of said trim elements;

determining, in said online mode of operation, one or more optimum trim bit sequences required to achieve a desired test result ~~results~~; and

permanently adjusting, in an offline mode of operation, one or more trim elements of the circuit device in accordance with the determined one or more optimum trim bit sequences;

said circuit device being connected to an external electrical measurement apparatus during said online mode of operation and being disconnected from said external electrical measurement apparatus during said offline mode of operation.

2. (canceled)

3. (currently amended) A method as in claim ~~2~~ 1, further comprising the step of generating and storing a data base representative of said one mor more optimum trim bit sequences.

4. (currently amended) A method as in claim ~~2~~ 1, further comprising the step of generating and storing a data base of information obtained in said ~~the~~ online mode of operation.

5. (currently amended) A method as in claim 3, further comprising the step of generating and storing a data base of information obtained in said ~~the~~ online mode of operation.

6. (original) A method as in claim 3, wherein said data base comprises a wafer map.

7. (original) A method as in claim 4, wherein said data base comprises a wafer map.

8. (original) A method as in claim 5, wherein said data base comprises a wafer map.

9. (currently amended) A method as in claim ~~1~~ 2, wherein, after the completion of trim bit sequences evaluation, said ~~the~~ online mode of operation is permanently disabled and said ~~the~~ offline mode of operation is permanently enabled.

10. (currently amended) A trimming circuit for use in trimming a circuit device containing trim elements, the trimming circuit comprising:

one or more trim elements;

one or more trim bit subcircuits, each of said trim bit subcircuits being associated with one or more trim elements; and

associated circuitry operative in online and offline modes of operation of said trimming circuit, said associated circuitry being further operative during said online mode of operation, for permitting the external application

of trim bit sequences to said circuit device.

11. (canceled)

12. (currently amended) A trimming circuit as in claim ~~11~~ 10, wherein said associated circuitry comprises a shift register for enabling external input or programming of said trim bit sequences.

13. (original) A trimming circuit as in claim 12, wherein said shift register comprises one or more trim bit subcircuits.

14. (original) A trimming circuit as in calim 13, wherein each one of said trim bit subcircuits is associated with a particular trim bit; and

each one of said trim bit subcircuits is associated with one or more trim elements.

15. (original) A trimming circuit as in claim 14, wherein each of said one or more trim bit subcircuits comprises a bistable flip-flop.

16. (original) A trimming circuit as in claim 14, wherein said one or more trim elements comprise one or more fuses.

17. (original) A trimming circuit as in claim 16, wherein said one or more fuses comprise one or more polysilicon fuses.

18. (original) A trimming circuit as in claim 16, wherein said one or more fuses comprise one or more metal fuses.

19. (original) A trimming circuit as in claim 14, wherein said one or more trim elements comprise one or more Zener diodes.

20. (original) A trimming circuit as in claim 14, wherein said one or more trim elements comprise one or more memory circuits.

21. (original) A trimming circuit as in claim 10, wherein each of said

one or more trim bit subcircuits comprises:

a current source connected to a selected one of upper and lower power supply rails;

a switch connected to a remaining one of said upper and lower power supply rails; and

a fuse connected between said current source and said switch.

22. (original) A trimming circuit as in claim 15, wherein each of said one or more trim bit subcircuits comprises two fuses, connected in series and to the one of said bistable flip-flop circuits associated with that trim element.

23. (original) A trimming circuit as in claim 10, wherein one or more of said trim elements are operative for permanently disabling said online mode of operation of said trimming circuit and for permanently enabling said offline mode of operation of said trimming circuit.